Navitas Recent Acquisitions: GeneSiC & VDD Tech August 15, 2022



Power IC

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Summary



Navitas has completed two exciting & strategic acquisitions to accelerate our mission to become the next-generation power semiconductor leader.



SiC Pioneer & Leader



Digital Isolators optimized for GaN / SiC

- High growth, highly profitable, accretive
- Highest performance, most robust, broadest portfolio of SiC FETs (650V - 6,500V)
- Fabless with robust supply chain
- Significant revenue in EV, solar, energy storage, wind, grid power & more
- Up to \$15B/yr new market potential

- Belgium-based, highly innovative start-up
- Digital isolators critical in all power systems
- Optimized for high-speed GaN and SiC
- Enables Navitas to offer complete power stage
- Up to \$1B/yr new market potential
- First products in expected in '23 and revenue growth expected in '24



GeneSic Sic Pioneers and Leaders



50+ years expertise in SiC

Power device design & process

22 company patents granted or pending; many innovation awards

Core team in device, process, test & product

1st commercial products introduced in 2011

Industry-leading SiC performance

Industry-leading robustness & reliability

Broadest range of SiC MOSFETs

Strategic relationships with multiple suppliers



Dr. Ranbir Singh, President

- Founded GeneSiC in 2004
- 25+ years dedicated to SiC
- Device design, process development and technology innovations
- Ph.D. and M.S. Electrical & Computer Eng, North Carolina State University, Bachelors Technology from Indian Institute of Technology, Delhi



Dr. Siddarth Sundaresan, VP Technology

- 14+ years with GeneSiC
- 23+ granted or pending patents on SiC MOSFET/Diode design and process technologies
- Ph.D. and M.S. Electrical & Computer Eng, George Mason University, dissertation on ultra-fast, hightemperature processing of SiC and GaN

Industry-Leading SiC Performance



Supplier	Resistance		Energy Loss				Figure-of-Merit (Low number is better)		
	R_{DS(ON)} @ 25°C (mΩ)	R_{DS(ON)} @ 175°C (mΩ)	E _{ON} @ 25A (μJ)	E_{OFF} @ 35A (μJ)	E OSS @ 800V (ய)	E _{ZVS} E _{OFF} -E _{OSS} (μJ)	Hard-Switching R _{DS} @ 175°C x (E _{ON} +E _{OFF}) (Ω-μ)	Soft-Switching R _{DS} @ 175°C x E _{ZVS} (Ω-μΙ)	
© GeneSiC™ SEMICONDUCTOR	40	57	600	80	34	46	38.8	2.6	
#2	40	68	600	80	40	40	46.2	2.7	
#3	40	80	850	390	35	355	99.2	28.4	
#4	40	71	550	150	35	115	49.7	8.2	
#5	45	85	520	65	29	36	49.7	3.1	

Lowest power loss at high temp, high speed

= Highest Efficiency, Energy Savings Small Size, Light Weight, Low System Costs!

Reference 1,200V SiC FET, 40-45m Ω devices; GeneSiC = G3R40MT12J; based on Navitas test result & competitive data sheet parameters.

Industry-Leading Robustness & Reliability



Industry's Highest 100% Tested Avalanche





Excellent Short-Circuit Withstand Time





Patented Trench-Assisted Planar SiC MOSFET

- Highly uniform in production
- Industry-leading robustness
- Highest 100% tested avalanche ratings
- World-class short circuit capability

Avalanche = capability to handle excess energy in fault condition **Withstand time** = survival duration in fault condition

Based on internal testing of 1200V SiC MOSFETs versus competitor products in same voltage, current range

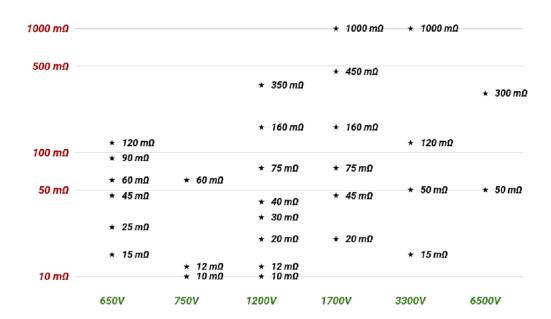
Broadest⁽¹⁾ SiC MOSFET Portfolio



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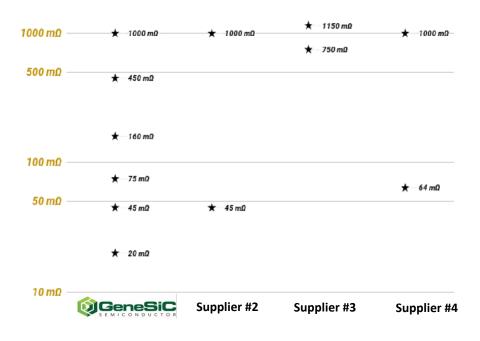


GeneSic 650V - 6,500V SiC MOSFETs



- 50+ SiC MOSFETs, array of standard packages
- Only supplier with 650V to 6,500V SiC MOSFETs

Most 1,700V SiC MOSFETs



Broadest industry offering for 1700V SiC MOSFETs



Note (1): based on GeneSiC voltage range of production released SiC MOSFETs compared to all publicly identified voltage ranges of other SiC suppliers.

Robust and Flexible Supply Chain





Finished SiC Wafer

World-Class SiC Devices

Tier-1, Low-Cost Packaging
Multiple, major suppliers qualified

SiC Wafer Substrate
Multi-sourced,
established suppliers

SiC Epi Layer
SiC Substrate

Showa

Wolfspeed

SiC Epi Layer

Multi-sourced reactors, scalable, highest-quality epi

Tier-1, Low-Cost Foundry

• 6"(150mm) wafers

xfab

- 25k wafers/month capacity.
- Automotive-rated Class-10
- Fully-Automated CMOS prod'n

90%+ yields
12+ combinations of substrate,
epi and foundry qualified
Industry highest die per wafer
Significant capacity expansion &
upside in 2022 / 2023
16-26 week lead-times

Over 500⁽¹⁾ Diverse & Synergistic Customers































































Energy Storage











































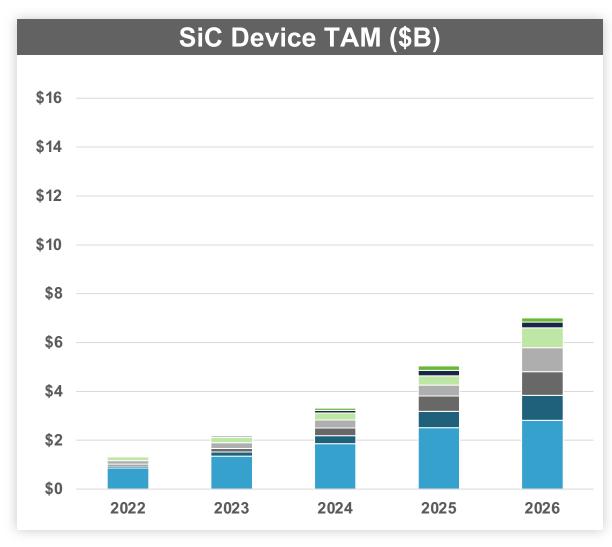


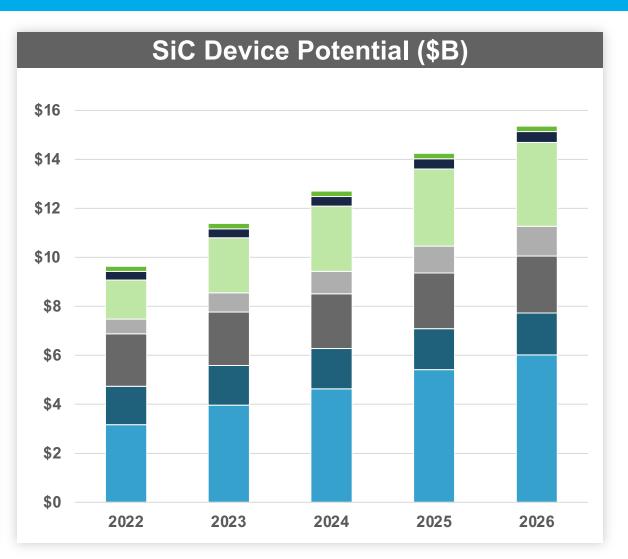




Fast-Growing SiC Power Semi TAM and Potential



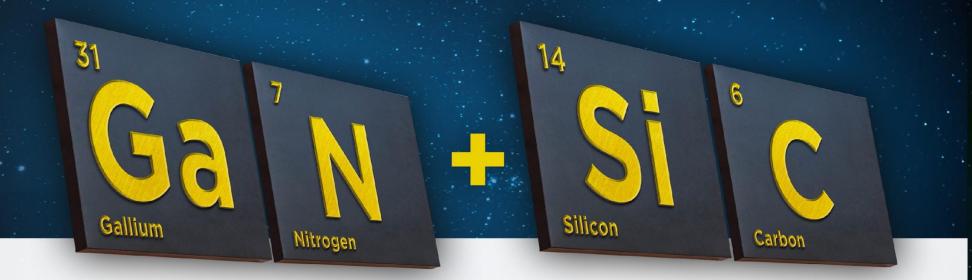




■ EV ■ Other ■ Industrial ■ Off-board chargers ■ Solar/ESS ■ Data Center ■ SiC Diodes

Source: Yole, DNV, IRENA, Fraunhofer ISE, IHS, Cisco, Hyperscale, Peer annual reports, Wall Street research.





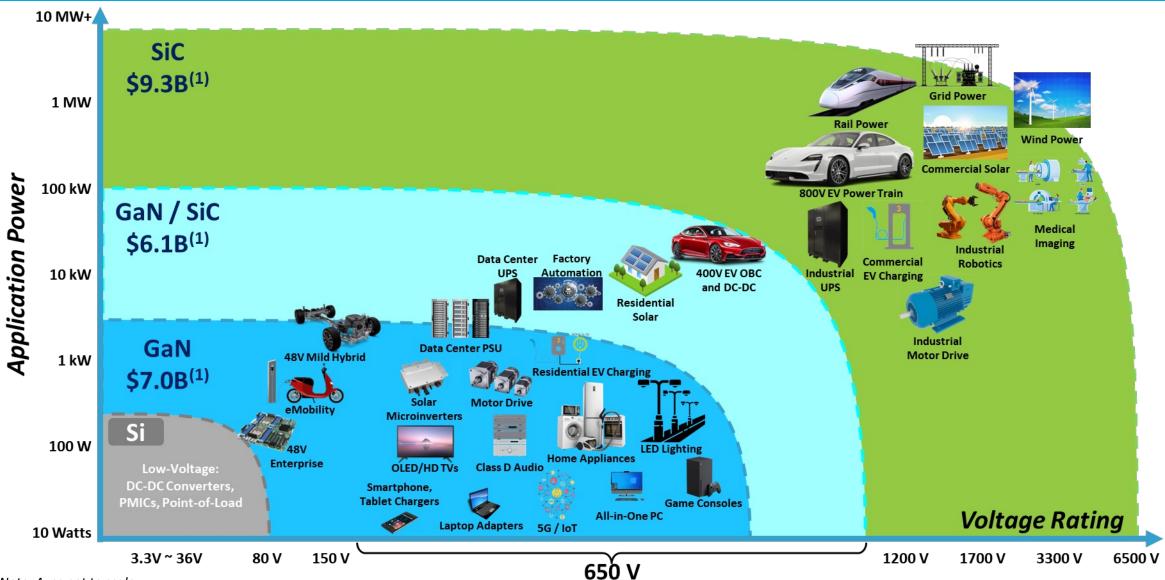




A Powerful Combination

GaN + SiC: The Future of Power Semis



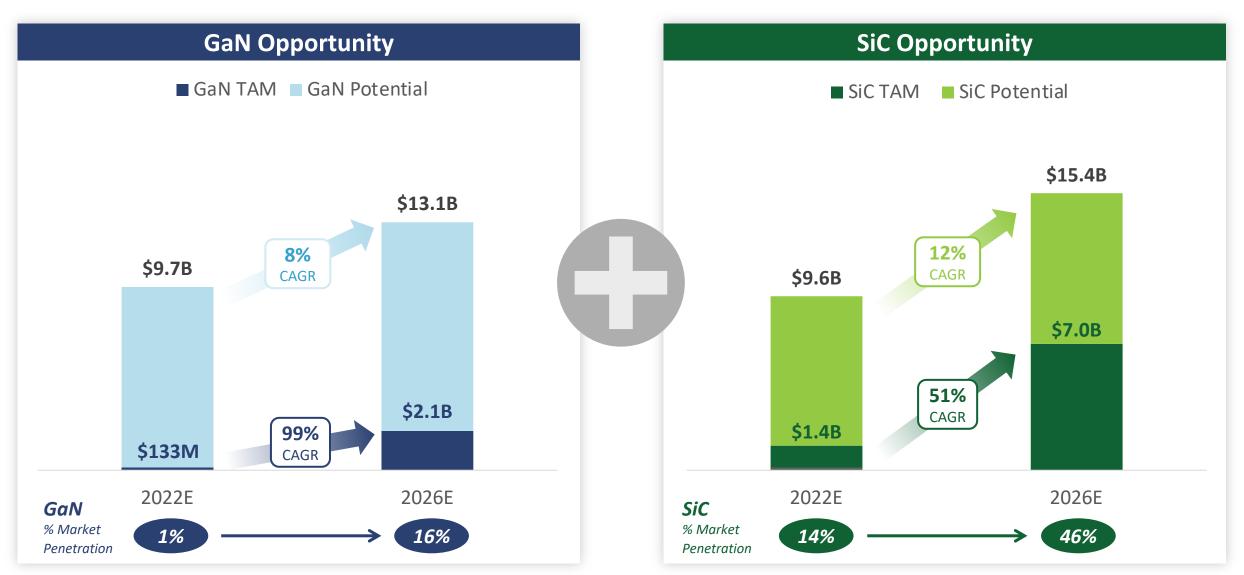


Note: Axes not to scale

Note (1): 2026E potential, Source: Yole, DNV, IRENA, Fraunhofer ISE, IHS, Cisco, Hyperscale, Peer annual reports, Wall Street research.

GaN and SiC Can Potentially Displace \$20B+ Market⁽¹⁾





Source: Yole, DNV, IRENA, Fraunhofer ISE, IHS, Cisco, Hyperscale, Peer annual reports, Wall Street research.

Note (1): 2026E includes \$6.1B in GaN / SiC overlap.

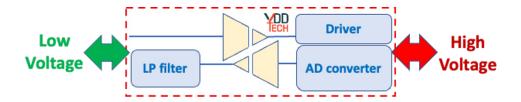


VUU ECH Critical, High-Speed Isolation



What are Digital Isolators?

- Critical circuits that interface low-voltage logic to high-voltage power
- Required in virtually all power systems for safety certifications





Phd. Vincent DESSARD

Founder, CEO, CTO

Serial Entrepreneur (Cissoid & X-Relsemi) High-T° & Analog design in Power Elec.



Phd. Amaid SAIB Senior Designer *Automotive* High-T° design

- Belgian start-up
- Uniquely talented in digital isolator technology

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IZL-100 Digital isolator	IZL-200 Analog isolator
	NZL-300 Transformer driver

Core IP Critical for GaN, SiC

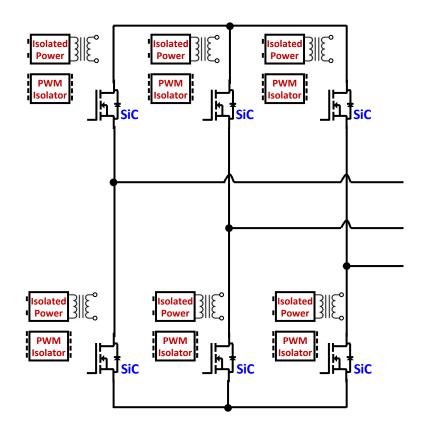
	VDD Tech	Supplier #2	Supplier #3	Supplier #4	Supplier #5
Galvanic Isolation	≥2.5kVRMS	✓	✓	✓	✓
dv/dt immunity	>200V/nsec	0	0	×	0
Low EMI	<0.5pF coupling cap	✓	×	×	×
Low-cost	Std CMOS	×	×	×	✓

GaN/SiC + Digital Isolators: A Perfect Match

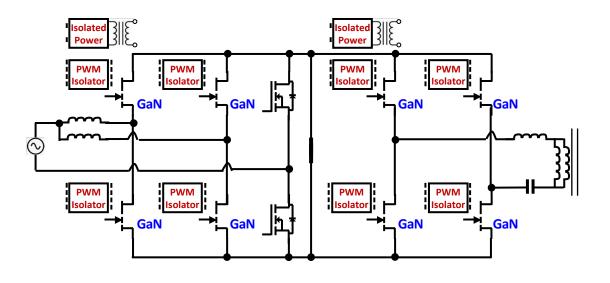


- Isolation is a mandatory safety barrier between low-voltage ICs and high-voltage GaN / SiC
- Navitas + VDD Tech = complete power stage integration & customer value

300 kW EV Traction Inverter



3 kW Data Center SMPS



- Up to 12 isolators per system, at \$0.25-\$1 each, up to \$4 per system
- Up to \$1B/yr market opportunity

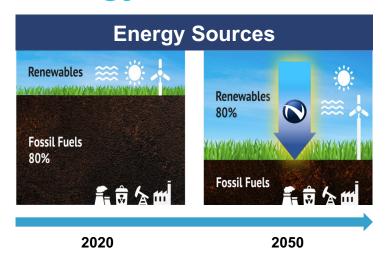
Source: Yole, DNV, IRENA, Fraunhofer ISE, IHS, Cisco, Hyperscale, Peer annual reports, Wall Street research.

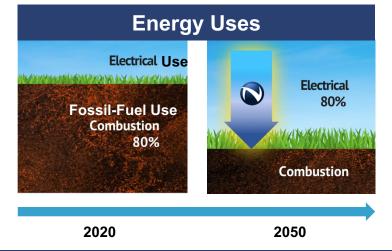
Electrify Our World™



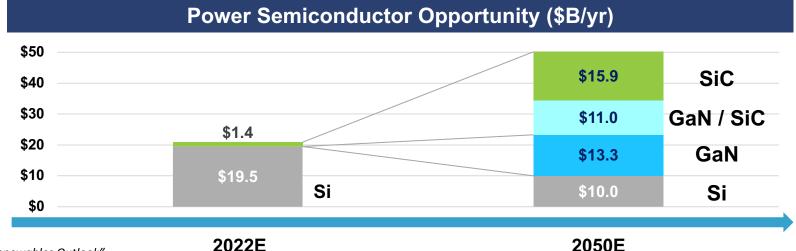
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Energy sources and uses are being electrified...





...creating a \$40B GaN + SiC opportunity by 2050



Fossil-fuel vs renewable ratios adapted from IRENA 2020 "Global Renewables Outlook".

Shift required to meet "Transforming Energy Scenario, 9.5 Gton target in 2050", per Paris Agreement's 1.5°C rise.

Market opportunity \$ from Yole Développement, 2020 and Navitas analysis.

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