



Breaking the AI Infrastructure Power Wall

Navitas 2.0 Completes the Grid-to-xPU Power Portfolio with Claros Acquisition

October 2026



Forward-Looking Statements and Legal Disclaimer

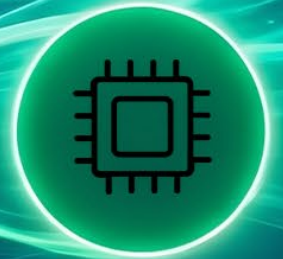
Any forward-looking statements contained in this presentation are included pursuant to the “safe harbor” provisions of the Private Securities Litigation Reform Act of 1995 and other federal securities laws. These forward-looking statements are intended to provide management’s current expectations or plans for the Company’s future operating and financial performance, based on assumptions currently believed to be valid. Words such as “anticipate,” “believe,” “estimate,” “expect,” “intend,” “plan,” “project,” “may,” “will,” “would,” “could,” “should,” and similar expressions are intended to identify forward-looking statements, although not all forward-looking statements contain these words. All forward-looking statements involve risks, uncertainties and other factors that may cause actual results to differ materially from those expressed or implied in the forward-looking statements. These statements, including statements regarding the anticipated benefits, synergies and prospects of the combined company following the completed acquisition of Claros, expected contributions to Navitas’ serviceable addressable market, technology roadmap, customer engagements, and financial model, are based on management’s current expectations and are subject to risks and uncertainties that could cause actual results to differ materially, including, among others: the risk that the anticipated benefits, synergies and cost savings of the transaction may not be realized within the expected timeframe or at all; the difficulties and costs of integrating the two businesses; significant transaction costs and/or unknown or inestimable liabilities; the effect of the transaction on the parties’ ability to retain and hire key personnel and to maintain relationships with customers, suppliers and other business partners; the diversion of management’s attention and resources from ongoing business operations; the impact of macroeconomic and market conditions, including economic downturns, international conflict, trade disputes and tariffs; and the other risks identified in the Company’s filings with the SEC. These forward-looking statements speak only as of the date of this release and the Company undertakes no obligation to update any forward-looking statement, except as required by applicable law.

Navitas®, GaNFast®, GeneSiC™, Claros™, SiCPAK®, GaNSafe®, DrGaN™, and the Navitas logo are trademarks or registered trademarks of Navitas Semiconductor Limited or affiliates. All other brands, product names and marks are or may be trademarks or registered trademarks used to identify products or services of their respective owners.



A Complete **Grid-to-xPU** Solution

Combining Navitas' GaN and SiC with Claros' IVR technology to deliver the full AI power chain.



Breaking the AI Infrastructure Power Wall

FROM GRID TO xPU BREAKING THE AI INFRASTRUCTURE POWER WALL

OUR IMPACT

2014

FOUNDED

\$3B

MARKET CAP
NASDAQ: NVTS

350M+

UNITS SHIPPED

450+

PATENTS ISSUED /
PENDING

US

HEADQUARTERED, R&D &
FOUNDRY

**AI
INFRASTRUCTURE**

FOCUSED

STRATEGIC PRIORITIES

1

Market Focus

AI Infrastructure (AI Data Center + Energy & Grid Infra) • High Perf Computing • Industrial. Pivoted away from Consumer

2

Technology Leadership

Pioneer in GaN, high-voltage & ultra-high voltage SiC, breakthrough IVR technology stack

3

Operational Efficiency

Resilient U.S.-based manufacturing and supply chain enabled by a foundry plus model and long-term strategic partnerships

4

Financial Discipline

Strengthen financial model and commitment to profitability through revenue scale and margin expansion

OUR TECHNOLOGIES



GaNFast™

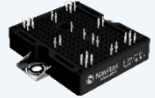


Gallium Nitride Power FETs & ICs

FAST • EFFICIENT • INTEGRATED



GeneSiC™

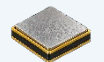


Silicon Carbide FETs & Modules

HV / UHV • ROBUST • RELIABLE



claros™



IVR Package & Embedded

HIGHLY INTEGRATED • HIGH DENSITY

Navitas 2.0 is focused on breaking the AI Infrastructure Power Wall, combining GaN, HV/UHV SiC, & IVR technologies to deliver higher efficiency, greater power density & increased performance from Grid-to-xPU.

Doubling SAM with a Focus on AI Infrastructure



Doubling Navitas' SAM to
over **\$8 billion**



Four focus markets

2030 SAM

AI INFRASTRUCTURE			\$6.9 B
	AI Datacenters	GaN / SiC / IVR	\$5.3 B
	Grid & Energy Infrastructure	HV / UHV SiC	\$1.6 B
	High Performance Computing	GaN	\$0.4 B
	Industrial Electrification	GaN / SiC	\$0.7 B

Grid & Energy Infrastructure

1

Grid to 800 VDC

SST • BESS • PCS
MV AC – 800 VDC



- ✓ Replaces bulky, lossy transformers while improving grid resilience
- ✓ Higher efficiency, power density & reliability
- ✓ Enables native 800 VDC with intelligent, bidirectional power flow & energy storage

Data Center

2

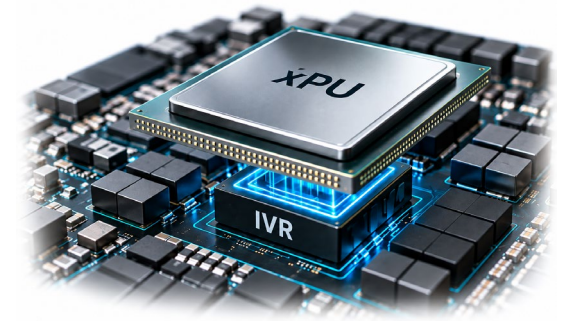
800 VDC to Core

HV IBC
High-Power Density DC-DC
800 VDC – 48 VDC – 6 VDC



- ✓ High-efficiency, high-density DC-DC
- ✓ 800V bus bar powers compute trays
- ✓ Reduces conversion stages and losses

LV IBC
Packaged & Embedded IVR
6 VDC – 0.7 VDC



- ✓ Last step power conversion to the xPU
- ✓ Ultra-fast transient response, very high current
- ✓ Highest efficiency and power density



**Higher
efficiency**

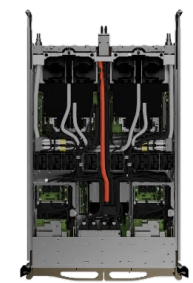
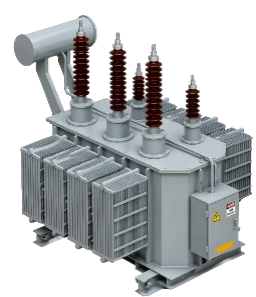
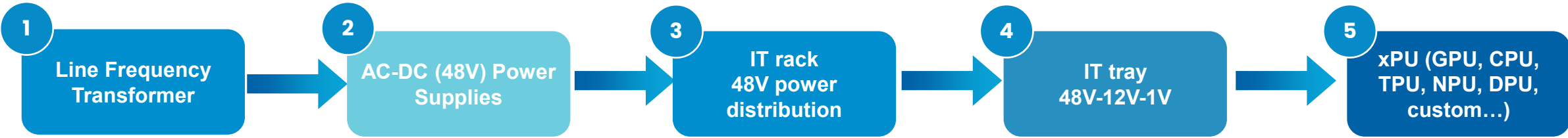


**Fewer
conversion stages**



**Greater
power density**

The 'AI Infrastructure Power Wall'



POWER WALL

Legacy transformers are bulky, inefficient & inflexible

POWER WALL

AC-DC PSUs are reaching their limits as AI power accelerates

POWER WALL

IT racks are constrained by power density & distribution losses

POWER WALL

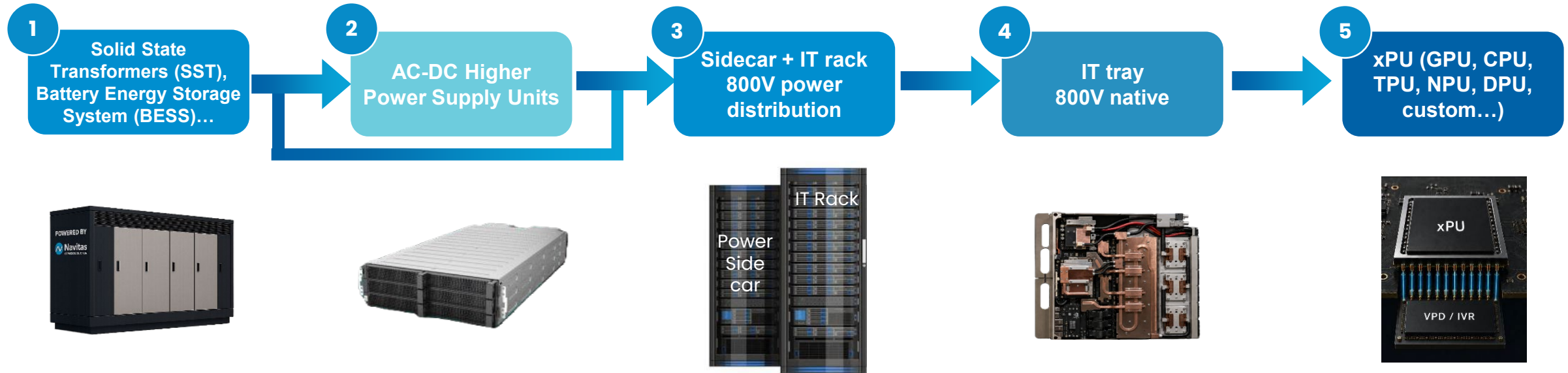
IT trays are limited by low voltage distribution losses

POWER WALL

xPUs performance restricted by lateral power delivery

THE POWER WALL As xPU power rises and rack increase power level and density, legacy conversion and lateral delivery create compounding losses, thermal constraints and power-density limits.

'Breaking the AI Infrastructure Power Wall'



BREAKING THE POWER WALL



SSTs convert Grid voltage to 800V DC, BESS improve grid resilience

BREAKING THE POWER WALL



High rack power drives 3-Phase high-density PSUs

BREAKING THE POWER WALL



AC-DC, DC-DC power shelves & BBUs move to sidecar with 800V output

BREAKING THE POWER WALL



800V server trays requiring high-density DC/DC closer to xPU

BREAKING THE POWER WALL



VPD & EPD, leveraging IVR technology, enables speed, efficiency, performance at <1V operation

BREAKING THE AI INFRASTRUCTURE POWER WALL

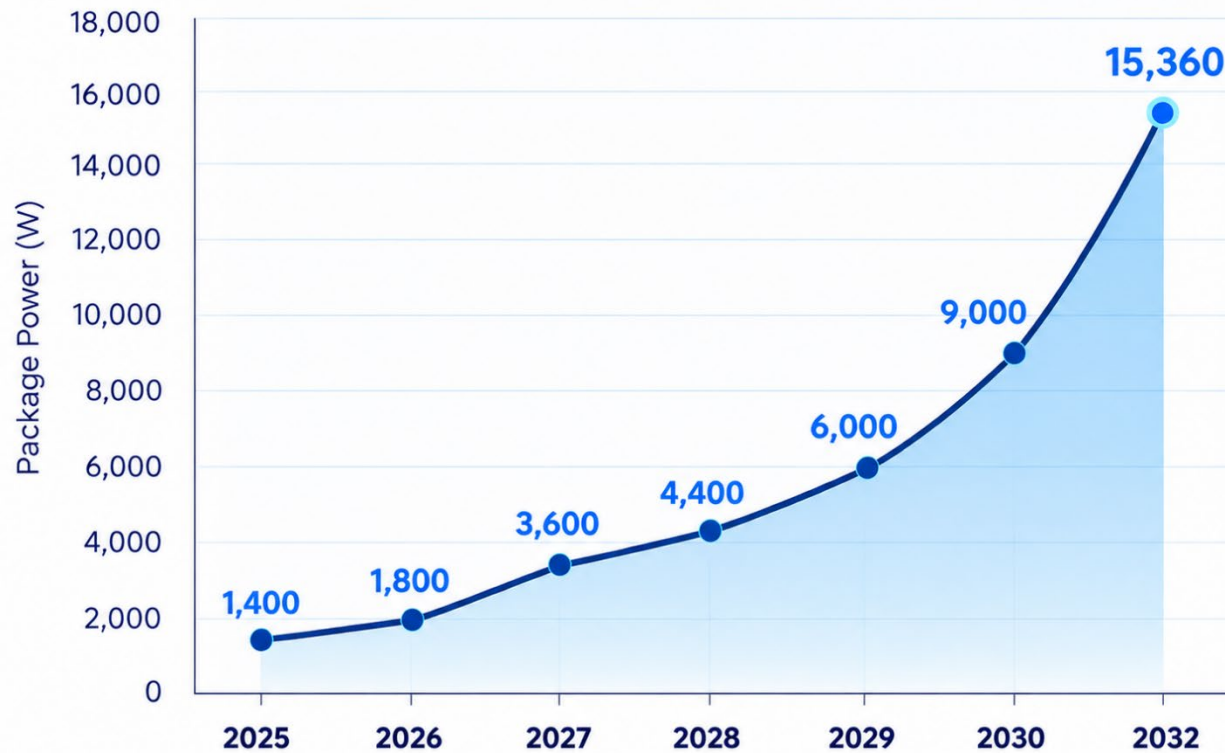
Breaking the power wall requires a simpler, higher-voltage centralized and higher current decentralized power architecture from Grid-to-xPU.

xPU Power Demand Is Outpacing Power Delivery



xPU Package Power Trend

(2025 – 2032)



xPU power trends indicate how **processor demand is rapidly increasing.**

VRM Power Wall: Lateral power delivery (LPD) cannot scale to deliver the power required by next-generation xPUs



Moore's Law limits

Traditional performance scaling through transistor miniaturization has reached physical limits.



Transmission & conversion inefficiencies

40% of power in data centers are lost, with the majority from the last few inches.



Packaging bottlenecks

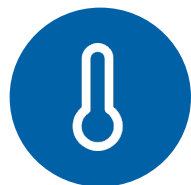
Current VRM packaging cannot efficiently manage increasing thermal loads, support higher power densities, & enable advanced cooling solutions.

**AI compute is outgrowing today's lateral power delivery.
The bottleneck Claros IVR technology stack is built to break.**



Efficiency losses

- Up to 30% power loss
- Creates a power-delivery bottleneck
- Limits xPU compute performance



Thermal Management

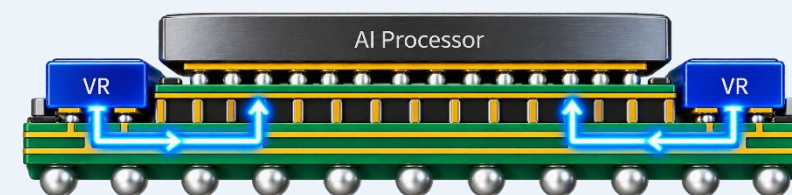
- Power losses become heat
- Increases xPU thermal load
- Drives more complex system cooling



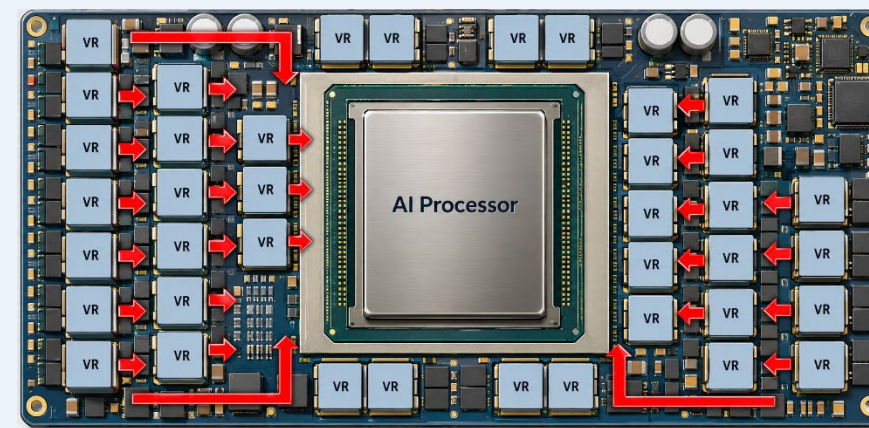
Board Space (Compute vs. Power)

- Power circuitry crowds out compute
- xPUs demand more board space & power
- AI compute demand accelerates (TFlops vs. Watts)

Lateral Power Delivery in VRM loses up to 30% power



Voltage regulators sit beside the processor



VRMs occupy significant board space. Energy is waste due to long distances (>1 inch)

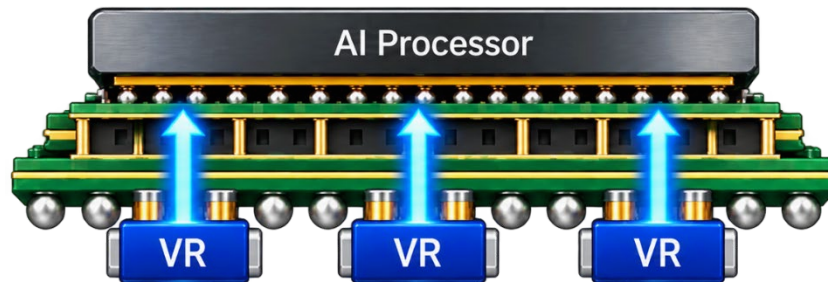
 Voltage Regulator Modules (VRM)

VPD & EPD Enable the Next Generation of xPU Power Delivery



Vertical Power Delivery (VPD)

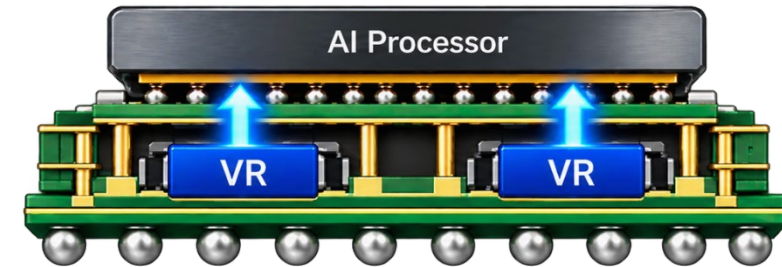
NEAR-TERM ARCHITECTURE



- VRM located directly below the xPU
- Short current path lowers inductance and supports higher current density
- Large external inductors and capacitors can be reduced

Embedded Power Delivery (EPD)

NEXT ARCHITECTURAL STEP



- VRM integrated into the xPU package or silicon substrate
- Lowest resistance & fastest transient response
- Optimized & configurable power delivery of individual xPU functional blocks

Increased xPU compute speed (TB, MHz)

Increased AI compute density (FLOPS/mm²), (FLOPS/Watt)

Increased power density (A/mm²)

claros™ – Advanced IVR Technology Stack Integrating Power, Control & Passives



1 DIGITAL CONTROL | Efficiency • telemetry • current sharing

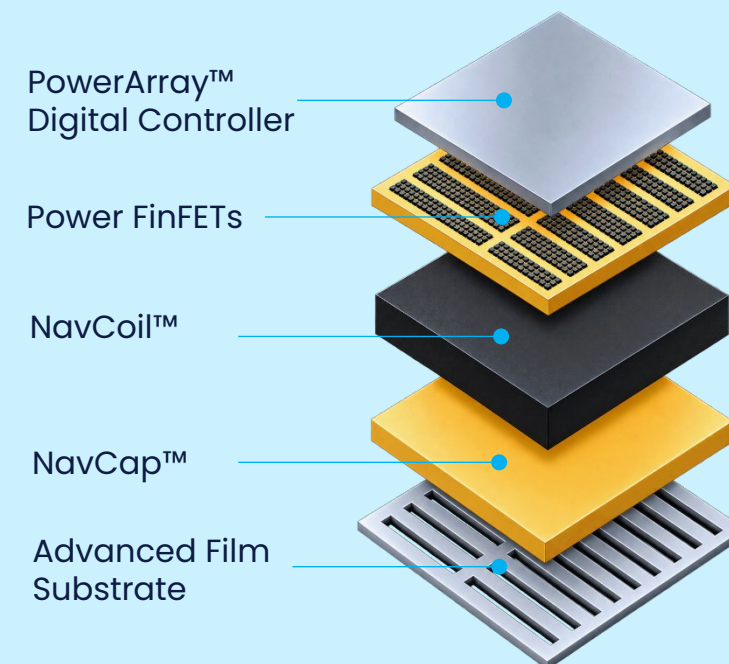
2 POWER DESIGN | ASIC / driver IC • power FETs

3 INTEGRATED PASSIVES | Silicon capacitors • inductors

4 ADVANCED PACKAGING | Compact integration of power + control + passives

5 SYSTEM ARCHITECTURE | Modular • scalable • faster time to market

Claros™ IVR Technology Stack



IVR combines control, power transistors, passives, packaging and system architecture into a tightly integrated IVR technology stack for next-generation xPU power delivery.

claros™ - IVR Technology Enables New Power Architectures and Two Product Paths



1 IVR TECHNOLOGY STACK

Claros™

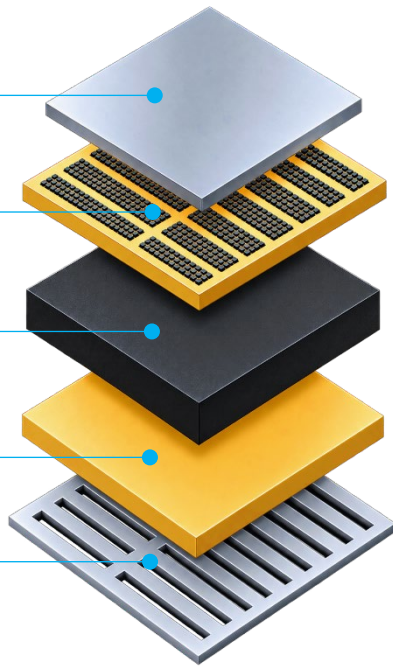
PowerArray™
Digital Controller

Power FinFETs

NavCoil™

NavCap™

Advanced Film
Substrate



2 POWER ARCHITECTURES

Vertical Power Delivery (VPD)

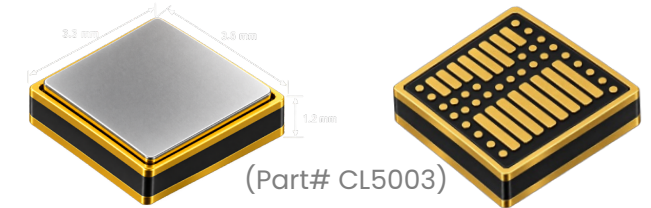
- Shorter power-delivery path
- Fast transient response
- High system power efficiency
- Scales with xPU power consumption

Embedded Power Delivery (EPD)

- Shortest power-delivery path
- Ultra-fast transient response due to extreme proximity
- Highest system efficiency
- Perfectly scales with xPU power consumption
- Less routing congestion for xPU

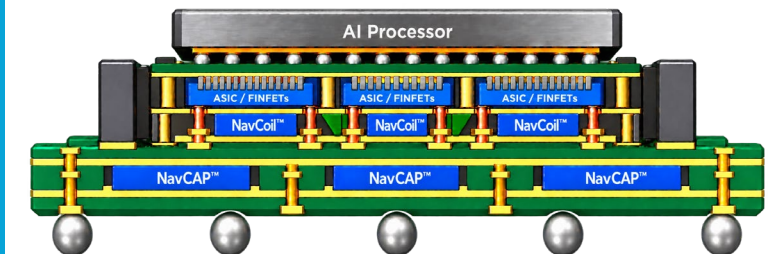
3 PRODUCTS

Packaged IVR (pIVR) – NavPIVR™



Complete IVR technology stack integrated into a single package

Embedded IVR (eIVR) – NavEIVR™



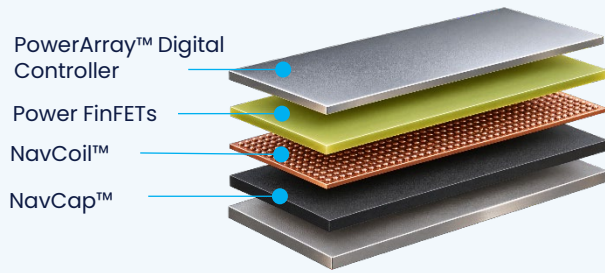
Embedded Si chilets and advance passives integrated directly into the xPU substrate

claros™ – Modular and Scalable Technology Built to Power Next-Generation xPUs



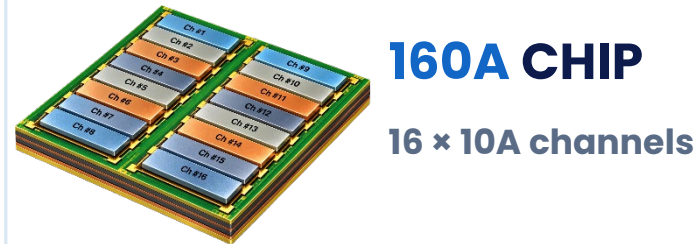
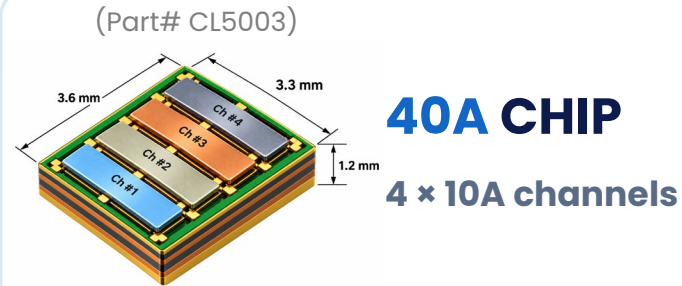
1 IVR TECHNOLOGY STACK

10A Building Block



Integrated power, control and embedded passives form a repeatable current-delivery cell.

2 CHIP SCALE



3 SYSTEM SCALE

PowerArray™

Same architecture, scalable and configurable to each xPU's current & power delivery requirements.

2,560 A 64 × 40A chips

10,240 A 64 × 160A chips



Modular architecture provides a common platform that can scale at chip and system level from tens of amps to >10 kA as xPU power requirements increase.

Delivering a Complete IVR Platform Built to Scale with AI



- Differentiated IVR platform spanning technology, architectures, products and system-level benefits
- IVR technology enables pIVR and eIVR products, supporting VPD and EPD architectures to move power conversion closer to the xPU

TECHNOLOGY

Key Leadership in Integration

- Power design: ASIC / driver IC + power FETs
- Advanced packaging and integrated passives
- PowerArray™ digital control, telemetry & system integration

ARCHITECTURES

Power Wall Delivery Breakthrough

- Vertical Power Delivery (VPD)
- Embedded Power Delivery (EPD)
- Moves power conversion closer to the xPU

PRODUCTS

IVR Product Portfolio

- Packaged Integrated Voltage Regulator (pIVR)
- Embedded IVR (eIVR)
- Common platform, multiple configurations

BENEFITS

Built to Scale with AI

- High current density for higher compute / watt
- Fast transient response for dynamic xPU loads
- Modular, scalable PowerArray™ architecture

Claros extends Navitas to the xPU with an integrated, scalable power-delivery platform.

Navitas & Claros Completes 'Grid-to-xPU' AI Infrastructure Power Portfolio



01 COMPLETE PLATFORM

Navitas + Claros create a complete Grid-to-xPU power platform

02 COMPLEMENTARY TECHNOLOGY

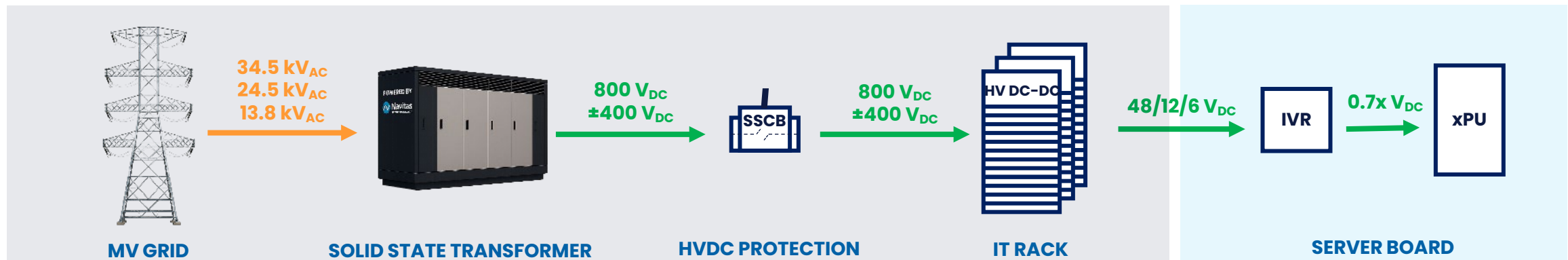
Leadership in GaN and HV/UHV SiC, combined with IVR enabling pIVR and eIVR for next-generation VPD and EPD architectures.

03 BREAKING THE POWER WALL

Breaking the AI infrastructure Power Wall enables the next generation of AI computing

FROM GRID TO xPU

BREAKING THE AI INFRASTRUCTURE POWER WALL



Navitas

claros

Navitas' GaN, SiC & IVR Portfolio Is Positioned Across Every Major AI Power Inflection



800V DC is inevitable as AI rack power and density increase, driving higher GaN + SiC content across four inflection points. IVR adoption enables the last step to high current demanding xPU

1

SiC in AC/DC PSUs

Higher rack power drives silicon-to-SiC replacement in high-density PSUs, even at 50V output.

SiC immediate growth replacing silicon in high power PSU

2

800V Power Sidecar

Power shelves and BBUs move to sidecar racks; 800V output adds SiC + GaN/SiC in DC/DC and BBU.

SiC + GaN content expands as moving to 800V

3

New AI Factory Power Architecture

Native 800V in compute trays via busbar.

GaN enables high-density DC/DC conversion closer to GPU/xPU loads.

xPU speed & power increases, requiring IVR solutions for highest performance, density, & efficiency.

GaN content accelerates with 800V bus bar

IVR adoption & growth, replacing traditional architectures

4

SST / Grid-to-Core

Solid-state transformers convert MVAC directly to 800V DC across data-center power distribution.

UHV SiC platform to modernize the grid

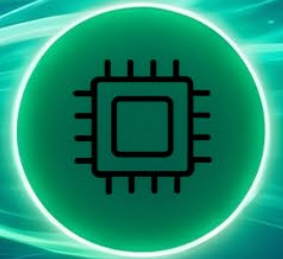
Content per system increases at every inflection





A Complete **Grid-to-xPU** Solution

Combining Navitas' GaN and SiC with Claros' IVR technology to deliver the full AI power chain.



Breaking the AI Infrastructure Power Wall



Navitas Semiconductor

Our Core Values



**Speed and
decisiveness**



**One team,
one mission**



**Trust, respect and
collaboration**



**Ownership and
accountability**



**Results
driven**